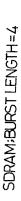


FIG.1A

SEAMLESS COMMANDING AND SEAMLESS DATA STAR



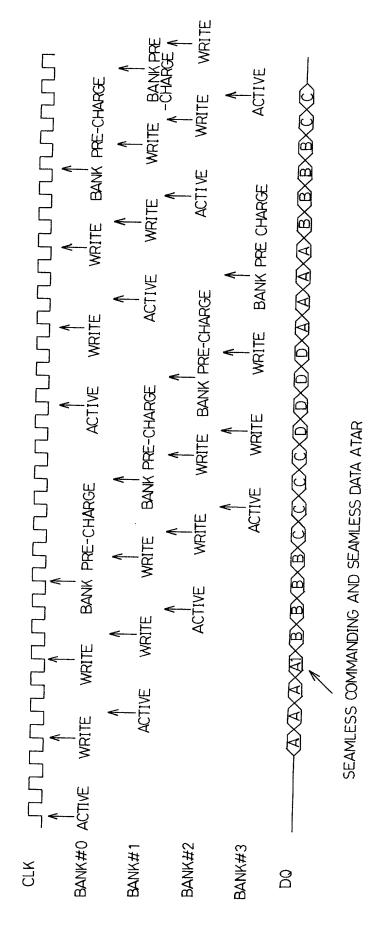
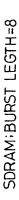


FIG.1B



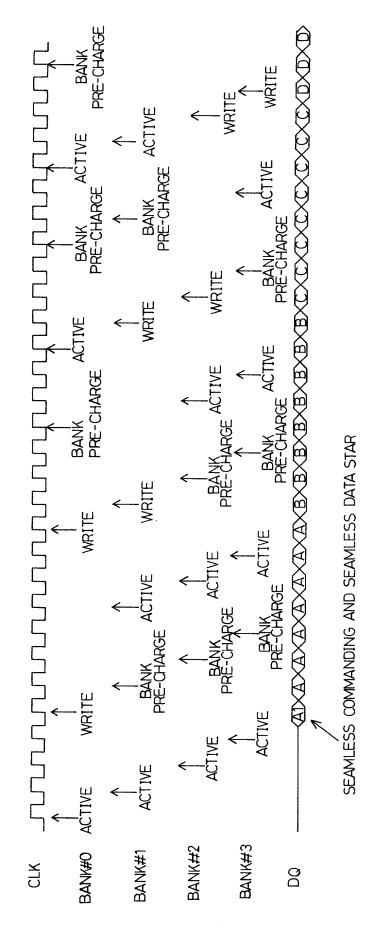


FIG.1C

SDRAM; LATENCY=2; BURST LENGTH=2;

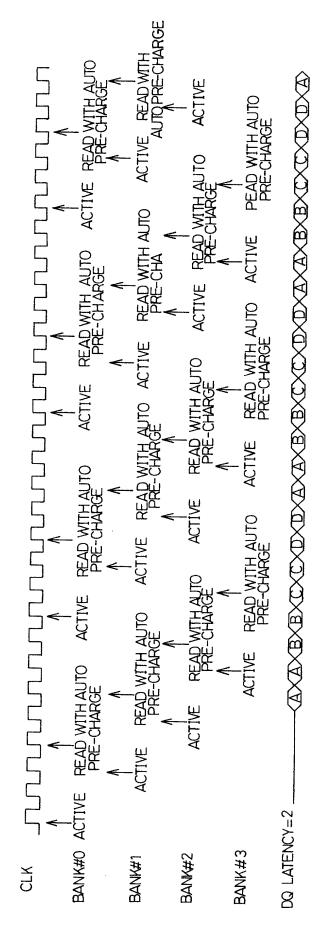


FIG. 2A

SDRAM:LATENCY=3;BURST LENGTH=2;

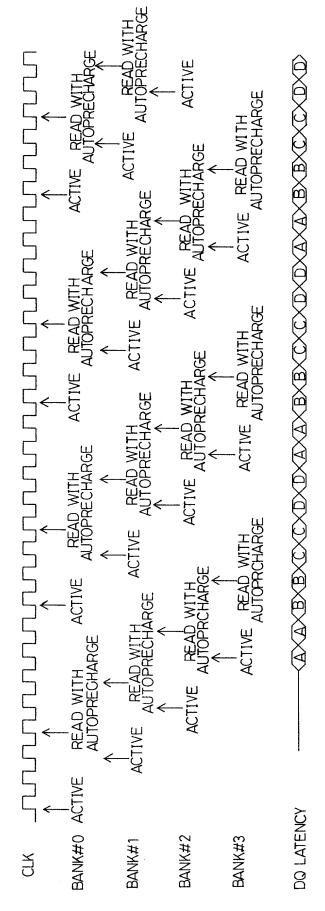
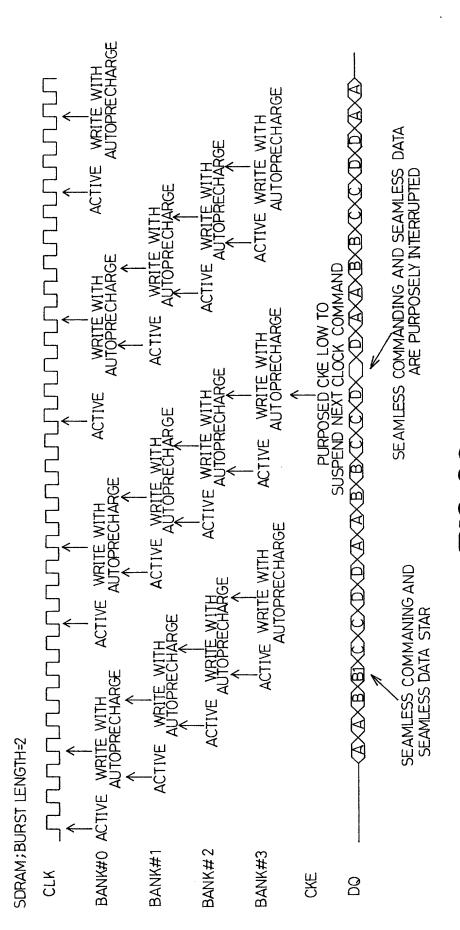


FIG. 2B



F16.2C

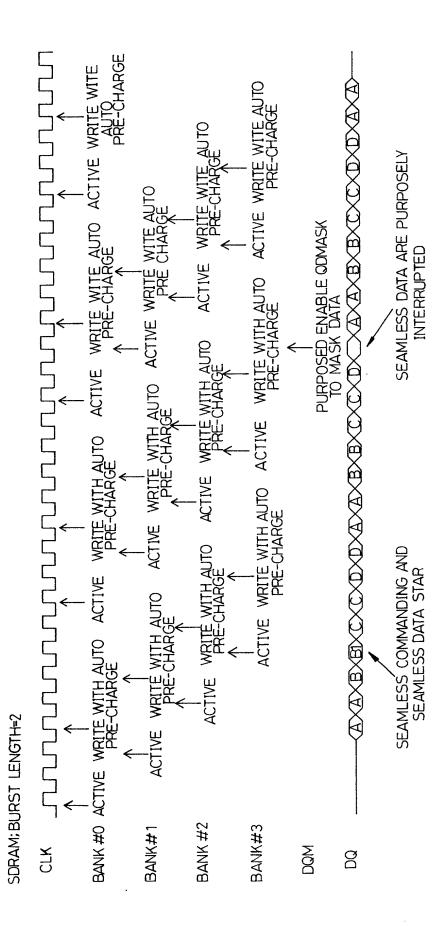


FIG.2D

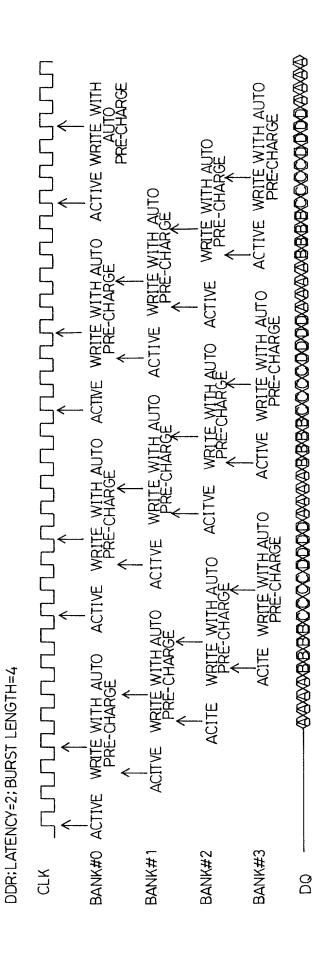


FIG.3A

DDR:LATENCY=2;BURST LENGTH=4

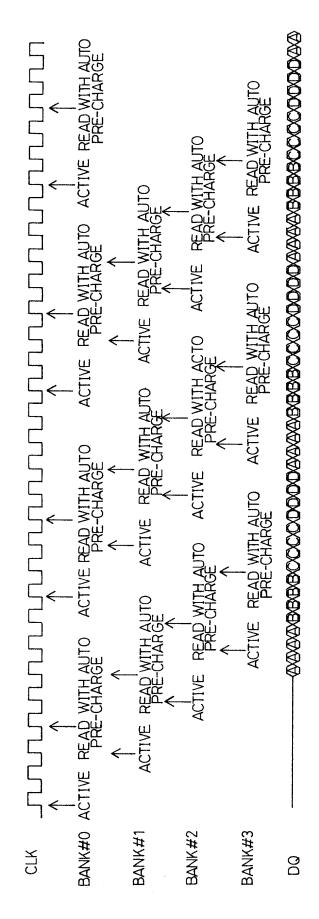


FIG.3B

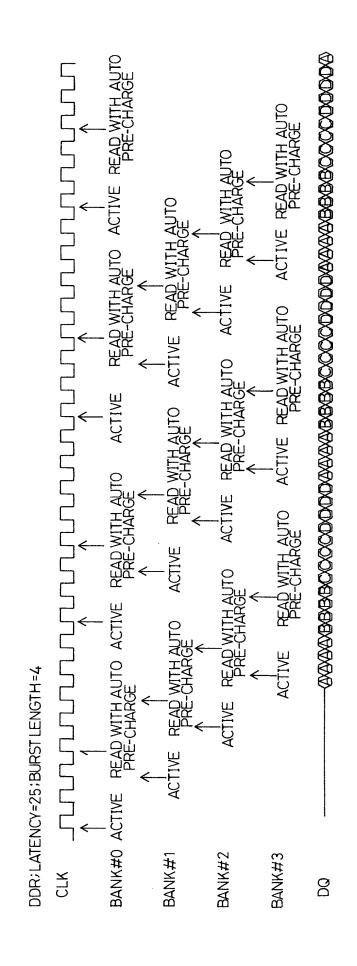


FIG. 3C

RDRAM: TRR=8 TCYCLE; TCWD=6 TCYCLE; TRTP=4 TCYCLE;

-SEAMLESS ROW PACKET COMMANDING→

SEAMLESS COL PACKET COMMANDING-

-SEAMLESS L.O. DATA PACKET-

FIG.4A

TRANSACTION A: a0 = {Da,Ba,Ra0} a1 = {Da,Ba,Ca1} a2 = {Da,Ba,Ca2} a3 = {Da,Ba,Ca3} a4= {Da,Ba,Ca4} TRANSACTION B: b0 = {Db,Bb,Rb0} b1 = {Db,Bb,Cb1} b2 = {Db,Bb,Cb2} b3 = {Db,Bb,Cb3} b4 = {Db,Bb,Cb4}	(Og (A)	al={Da,Ba,Cal}	37= (Da Ra (37)		
TRANSACTION B: b0={Db,Bb,R	Q		ac (24, 24, 242)	a3 = {La, ba, (a3)	44= {La,ca,La4}
		b1 = {Db,Bb,Cb1}	b2={Db,Bb,Cb2}	b3 = {Db,Bb,Cb3}	b4 = {Db,Bb,Cb4}
TRANSACTION C: c0={Dc, Bc, Rc0}	PCO}	c1 = {Dc,Bc,Cc1}	c2={Dc,Bc,Cc2}	c2 = {Dc, Bc, Cc2} c3 = {Dc, Bc, Cc3}	c4={Dc,Bc,Cc4}
TRANSACTION D: d0={Da,Bd,R	(SP2)	Da, Ba, RaO}	d2 = {Dd,Bd,Cd2} d3 = {Dd,Bd,Cd3}	d3 ={Dd,Bd,Cd3}	d4={Dd,Bd,Gd4}
TRANSACTION E: e0={De,Be,Re0} e1={De,Be,Ce1} e2={De,Be,Ce2} e3={De,Be,Ce3}	Re0}	el ={De,Be,Ce1}	e2={De,Be,Ce2}	- 1	e4={De,Be,Ce4}

RDRAM: TRR=8 TCYCLE: TCAC=8 TCYCLE: TRAS=20 TCYCLE: TRDP=4 TCYCLE:

ROWZ: (ACT aO)[[[[[]]]]ACT 60|PRER ACT 40|PRER ACT 40|PRER ACT 40|PRER ACT 60|PRER ACT 60|PRER ACT 60|PRER -SEAMLESS ROW PACKET COMMANDING→

F—SEAMLESS COL PACKET COMMANDING—→

COL4- WWWWWWWW at RD at RD by RD by RD cri RD cz RD dri RD at RD at RD at RD by RD c3

SEAMLESS L.O. DATA PACKET-

F16.4B

SDRAM:BURST LENGTH=4

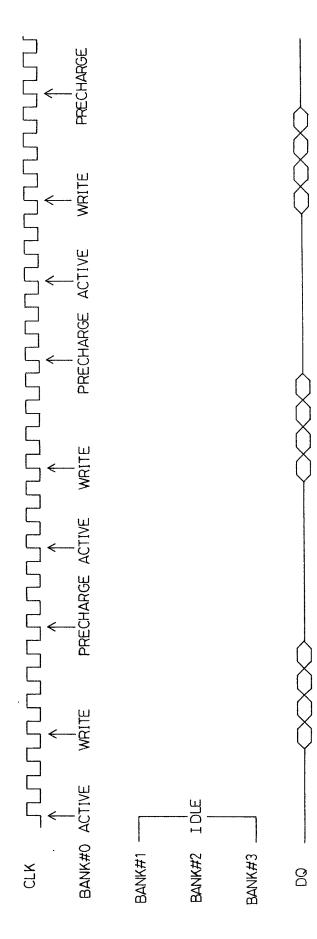


FIG.5 PRIOR ART

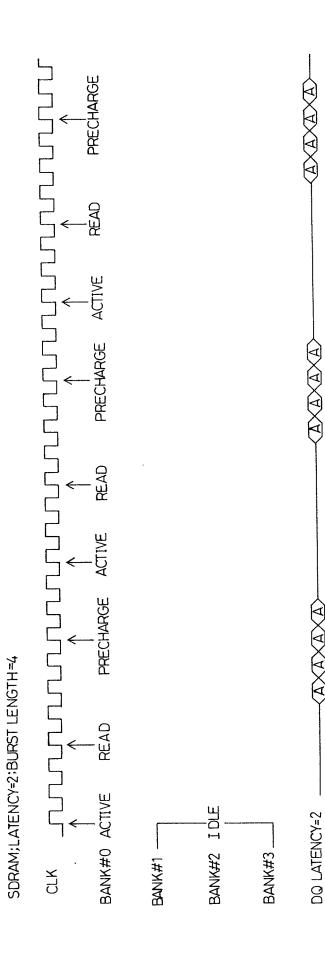


FIG.6A PRIOR ART

SDRAM;LATENCY=3:BURST LENGTH=4

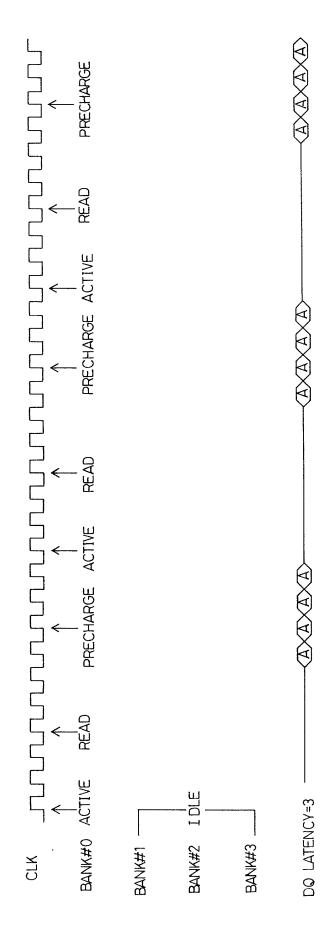


FIG.6B PRIOR ART

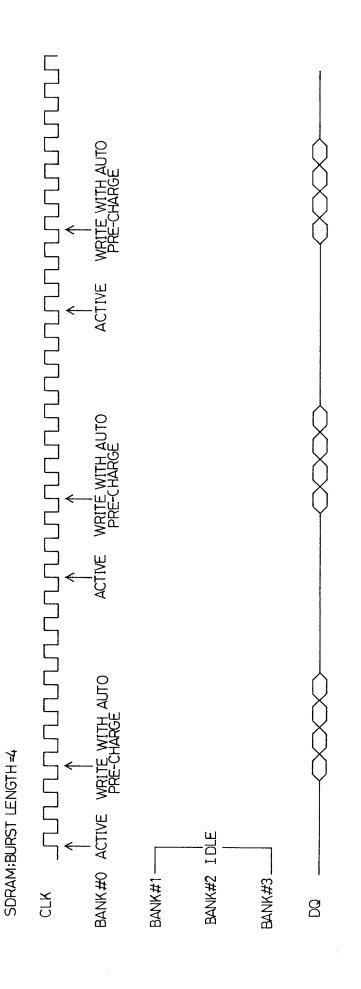


FIG.7 PRIOR ART

SDRAM; LATENCY=2; BURST LENGTH=4

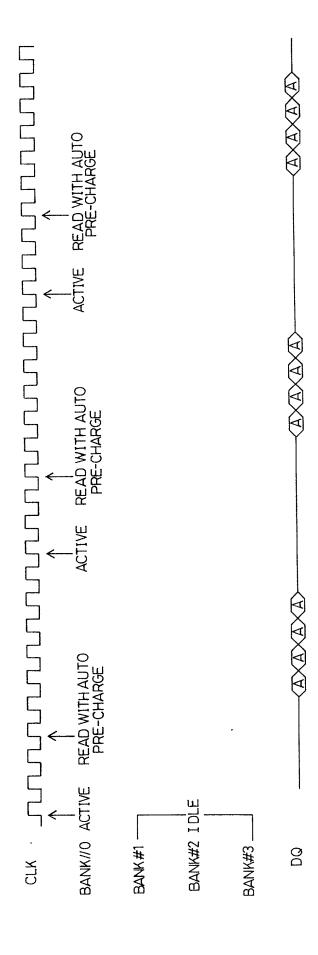
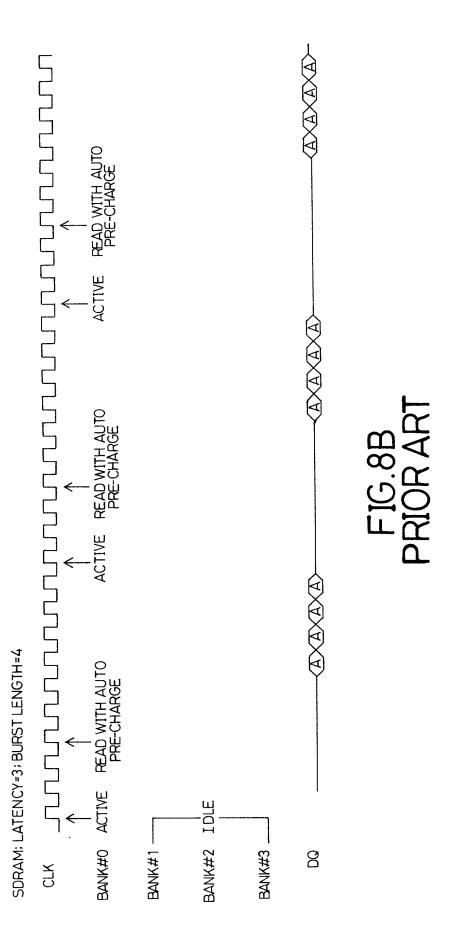
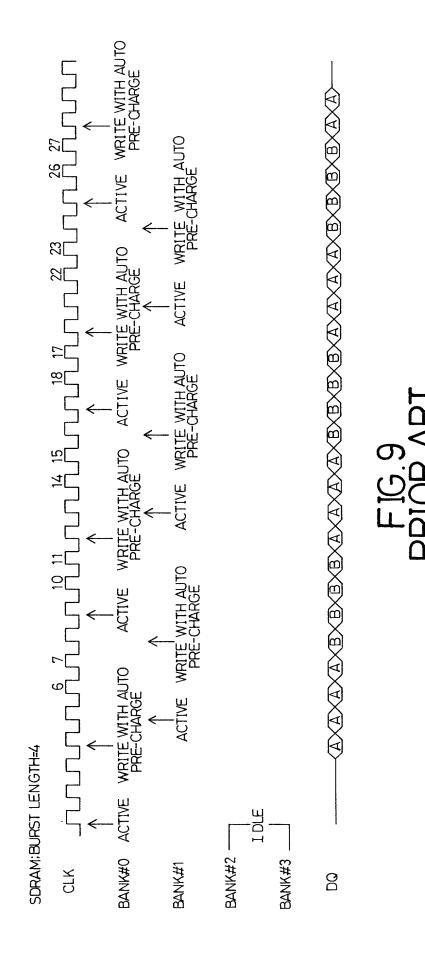


FIG. 8A PRIOR ART





SDRAM;LATENCY=2;BURST LENGTH=4

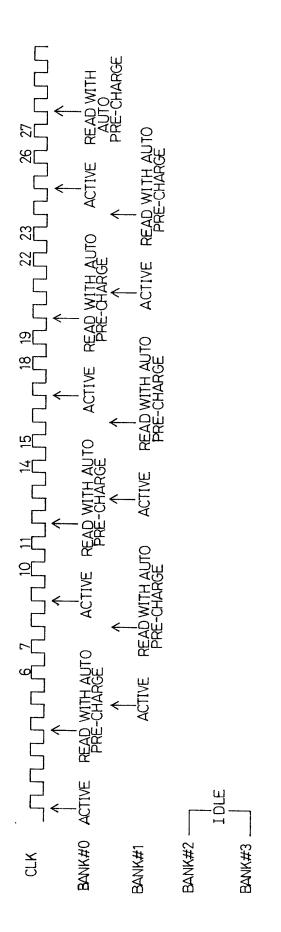


FIG.10A PRIOR ART

8

SDRAM; LATENCY=3; BURST LENGTH=4

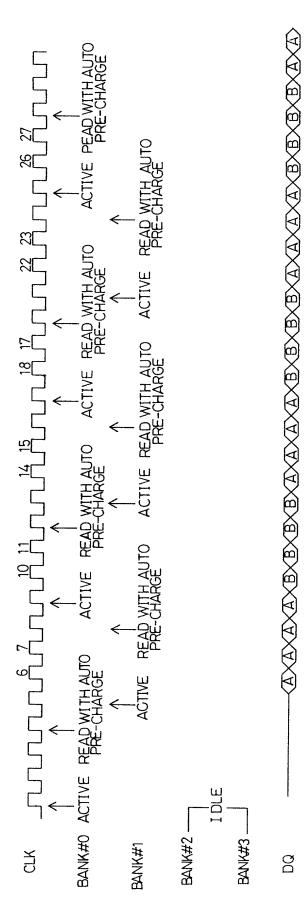


FIG.10B PRIOR ART

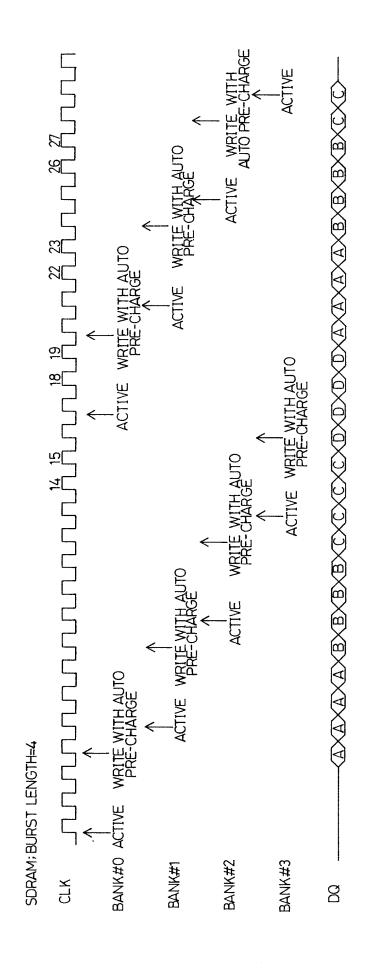


FIG.11 PRIOR ART

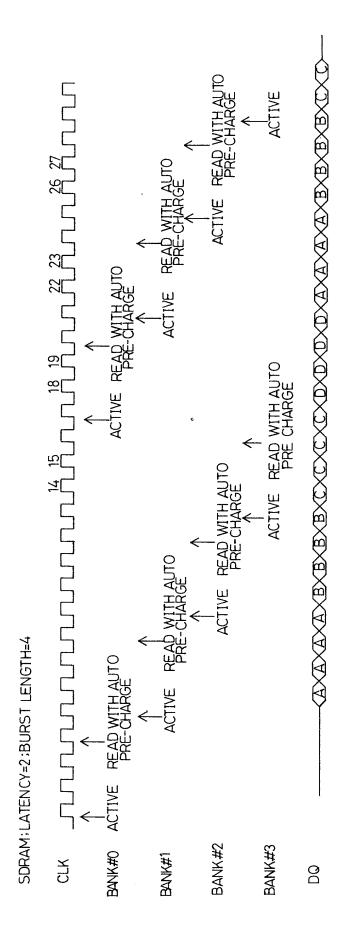


FIG.12A PRIOR ART



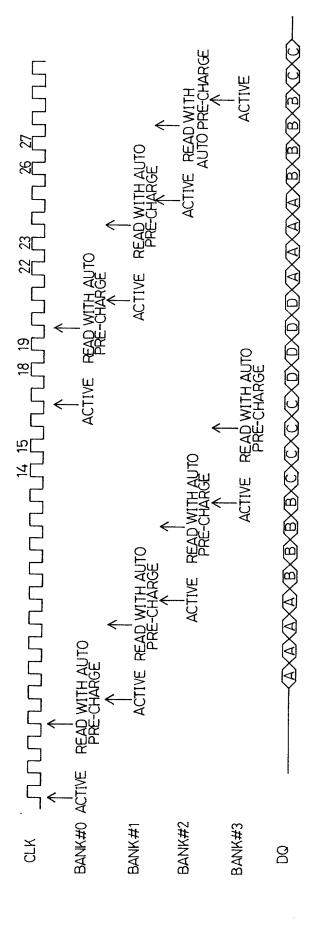


FIG.12B PRIOR ART